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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,579	11/15/2001	Akira Ohta	57454-278	7330

7590 03/31/2004

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EXAMINER	
JONES, STEPHEN E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,579	OHTA ET AL.	
	Examiner	Art Unit	
	Stephen E. Jones	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-12* is/are pending in the application.

4a) Of the above claim(s) *6-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-3 and 5-12* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/3/04 has been entered.

Election/Restrictions

1. Claims 6-12 remain withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makino et al (of record) in view of Krauss et al. ("Solid State Radio Engineering") (of record).

Makino (Figs. 1, 2 and 7) teaches a microwave (i.e. high frequency) amplifier including: a nonreciprocal isolator device (1) having an input impedance lower than the output impedance (see Fig. 2); a substrate (51); an amplifier (15) receives an input signal; an output matching circuit (16) receives the amplified signal; a filter element (6) is provided with the isolator device (1) on the substrate (51); the filter (6) receives the output from the output impedance matching circuit (16) and has a cutoff frequency fc (see Col. 4, lines 62-66) thus the filter passes a selected frequency; the filter includes an inductor (L) on the signal line and first and second capacitors between respective nodes on each side of the inductor and ground forming two signal lines to ground having capacitors on the lines (see Fig. 1); the output of the isolator is 50 ohm and the output of the amplifier (and input of the isolator circuit) is in the range of 2 to 12.5 which includes values in the range 3 to 30 ohms as claimed (Claim 3); and the cutoff frequency is between .75 fo and 2 fo (see Col. 4, lines 33-35) which includes values between fo and 2fo (Claim 5).

However, Makino does not explicitly teach a harmonic processing circuit for matching of harmonics included in the output of the amplifier (Claims 1, 2). Also, Makino

does not explicitly teach that the substrate (51) has a ground on the bottom surface and the amplifier has a ground, and further that via holes connect the capacitors (C in Fig. 1) through the substrate to ground (formerly Claim 4, now Claim 1). It should be noted that Makino does appear to show pads including via holes on the top of the substrate in Fig. 7 including some pads/holes connected to the amplifier but does not describe them in the specification.

Krauss et al. teaches that output matching circuits are used to reduce harmonics.

It would have been considered obvious to one of ordinary skill in the art to have additionally used the output matching circuit of Makino et al. as a harmonics reduction circuit (i.e. a harmonic processing circuit for matching harmonics) such as suggested by Krauss, because it would have provided the advantageous benefit of reducing the harmonics to an acceptable level (see Krauss page 418), thereby suggesting the obviousness of such a modification.

Also, it would have been considered obvious to one of ordinary skill in the art to have the capacitor lines of the filter element (6) (as shown in Fig. 1) and the amplifier of Makino to have been connected/extended through vias to a ground plane on the bottom of the substrate, because it is well-known to provide a ground plane on the bottom of main substrates including via holes from the top of the board to the bottom ground plane for grounding circuitry, and would have provided the advantageous benefit of a common ground connection between the isolator ground and the circuit board substrate ground as well as the other circuit components.

Also with respect to claim 1, it is an obvious consequence that the combination of Makino and Krauss provides a "proper output load of harmonics" since the matched from source to load condition is the most efficient condition, and the combination can be considered improved since the circuit would be more efficient than an unmatched circuit. Thus the claim language is met.

Response to Arguments

5. Applicant's arguments filed 3/3/04 have been fully considered but they are not persuasive.

Applicant argues the obviousness rejection of the capacitor lines of the filter element 6 and amplifier of Makino being connected/extended through vias to a ground plane on the bottom of the substrate because neither Makino or Krauss suggests the features.

This argument is not convincing. As pointed out in the last office action, the Maruhashi et al. reference was provided as evidence which teaches providing ground connections for electrodes on the top of a substrate by means of vias connecting to a bottom ground plane (e.g. Fig. 2). Certainly, with the evidence provided by Maruhashi it would have been obvious to have made the Makino connections of the capacitors (C) of the two signal lines that are connected to ground (e.g. see Fig. 1) by means of a well-known via to a ground plane on the bottom of the circuit board, and as noted in the rejections, Makino also appears to show pads including via holes on the top

of the substrate in Fig. 7 including some pads/holes connected to the amplifier but does not explicitly describe them in the specification.

Applicant also argues that the Krauss teaching that output matching circuits are used for reducing harmonics is not sufficient to suggest that the output matching circuit 16 of Makino is a harmonic processing circuit, and provides no reason to conclude that the harmonic processing circuit would be on the same substrate with the amplifier and filter element.

This argument is not persuasive. Processing of harmonics (as in the present claims) in its broadest interpretation includes reducing harmonics since reducing harmonics is a form of "processing". With regard to the harmonics processing circuit location, as shown in Fig. 7 of Makino, the entire circuit including the filter, matching circuit, isolator, and amplifier are all on the same substrate (51), thus it would not have been practical to have the harmonics processing circuit anywhere other than on the circuit board 51, especially since the harmonics processing circuit is associated with the matching circuit as described by Krauss.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 571-272-1762. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen Jones
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Art Unit 2817

SEJ